This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-3 (Cancelled)

4. (Currently amended) A method for fabricating a mask ROM comprising the steps of:

providing a substrate where a memory cell array region and a segment select region are defined;

forming an element isolating film at an outer portion of the memory cell array region and an isolating pattern at the outer portion of a buried layer formation region in the segment select region, the buried layer formation region defining a region for a portion of a buried layer to be formed in the segment select region, and the isolating pattern isolating the portion of buried layer from ~~of the memory cell array region and at the outer portion of a buried layer formation region of~~ the segment select region;

forming ~~a plurality of~~ the buried layer[s] aligned over the resultant structure in a first direction by a predetermined interval ~~and surrounded by the isolating pattern~~; and

forming a ~~plurality of~~ gate[s] aligned in a second direction to cross the buried layer[s] in an orthogonal direction.

5. (Original) The method according to claim 4, wherein the step for forming the element isolating film and the isolating pattern comprises the steps of:

forming first and second trenches at the outer portion of the memory cell array region and at the outer portion of the buried layer formation region of the segment select region;

forming an insulating layer on the substrate having the first and second trenches; and

etching the insulating layer.

6. (Original) The method according to claim 5, wherein the insulating layer is etched according to an etch back process or a chemical mechanical polishing process.

7. (Original) The method according to claim 4, wherein the step for forming the buried layers comprises the steps of:

forming a pad oxide film and a nitride film on the substrate having the element isolating film and the isolating pattern;

forming a mask pattern on the nitride film to cover the buried layer formation region;

exposing the substrate by removing the nitride film and the pad oxide film by using the mask pattern;

implanting impurities to the exposed substrate by using the mask pattern and the isolating pattern as a blocking mask; and

removing the mask pattern.

8. (Original) The method according to claim 4, wherein the first and second trenches have a depth of 3000 to 4000 .ANG. from the surface of the substrate.

9. (Original) The method according to claim 4, further comprising the steps of:

forming a protective film on the substrate having the gates;

forming a contact to partially expose the buried layer of the segment select region, by etching the protective film; and

forming a bit line to cover the contact.

10. (New) A method for fabricating a mask ROM comprising the steps of:

providing a substrate where a memory cell array region and a segment select region are defined;

forming a first trench isolation for separating the segment select region from the memory cell array;

forming a second trench isolation;

forming a first buried layer aligned over the resultant structure in a first direction by a predetermined interval;

forming a second buried layer separated from the first buried layer by the second trench isolation; and

forming a gate aligned in a second direction to cross the first buried layer in an orthogonal direction.